DIAMOND SYSTEMS CORPORATION

GPIO-MM-12 User Manual

FPGA-based PC/104 Counter/Timer and Digital I/O Module

User Manual v1.00

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Table of Contents

Figures

General Description

Overview

The GPIO-MM-12 is a PC/104 board featuring 48 Digital I/O (DIO) lines, 10 16-bit counter/timers, 8 bits of TTL input, 8 bits of TTL output, and software-controlled interrupt capability. The DIO and counter/timer functions are implemented in FPGA cores, emulating dual 82C55A PPI and dual CTS9513 counter/timer chips.

A 50-pin I/O header provides for external DIO connections. Direction on all ports is selected by programming control registers in the FPGA. All I/O lines are buffered with transceivers, whose directions are controlled by logic that responds to the direction control values written to the registers. Each line is capable of sinking 64mA in a logic low state or sourcing 15mA in a logic high state. The board requires only +5V for operation.

DIO headers are organized to allow direct interfacing to OPTO-22s isolated I/O racks, including the G4 series, the PB16-H, -J, -K, -L, PB8H, and the PB24HQ. These racks and I/O modules allow up to 3000 VRMS isolation between the computer and the user's signals. All control signals, power, and ground on the DIO header match the corresponding signals on these I/O racks, so a single 50-pin ribbon cable, such as Diamond Systems' C50-18, is all that is needed to make the connection.

The FPGA counter/timer cores provide an additional 8-bit TTL output port with up to ±4 mA per bit and a separate 8-bit TTL input port. Both ports can be operated in bit or byte mode.

The counter/timer provides ten extremely versatile counters with a wide variety of features, including up or down counting, binary or BCD counting, single or repetitive counting, edge or level gating, output pulse or toggle capability, alarm comparator circuitry, and software or hardware retriggering.

All counter features are programmable through software. In addition, an internal series of frequencies is provided, which may be used as internal count sources. The counter/timers can be used to generate retriggerable one-shots, timed pulses, and square waves of variable duty cycle, and to count pulses, measure time intervals between pulses, and measure the frequency and period of a periodic waveform.

The GPIO-MM-12 provides access to interrupt levels 3-7, 10-12 and 15 on the PC bus for real-time background applications. Interrupts provide a means for transferring data into or out of PC memory under external control. Using interrupts allows "background" operation, where I/O can be performed while the PC is executing another task, such as running an unrelated applications program. This feature is useful for performing I/O at a controlled rate, since a counter output can be used to drive the interrupt request pin on the I/O header at a periodic rate for a user-supplied interrupt service routine that performs whatever function is necessary in response to the interrupt.

Digital I/O Features

- Dual 82C55A Parallel Peripheral Interfaces (PPI) logic implemented in FPGA cores.
- Each 82C55A has three 8-bit I/O ports for a total of 48 DIO lines, which connect to a 50-pin header for external connections.
- Port direction and operation is selected through software programmable control registers.
- All lines are buffered with transceivers.

Counter/Timer Features

- Dual CTS9513 counter/timers logic implemented in FPGA cores.
- A 40MHz clock input, providing higher precision timer functions.
- Ten 16-bit programmable up/down counters with sophisticated timing logic:
  - Up or down counting.
  - Binary or BCD counting.
  - Single or repetitive counting.
  - Edge or level gating.
  - Output pulse or toggle capability.

    - Alarm comparator circuitry.
    - Software or hardware retriggering.
- Timing functions are software programmable, using control registers.
- 8-bit TTL input and 8-bit TTL output ports, which can operate in bit- or byte mode.
- An interrupt line for generating interrupts to the CPU.
- An external 50-pin header for connecting to the counter/timer features.

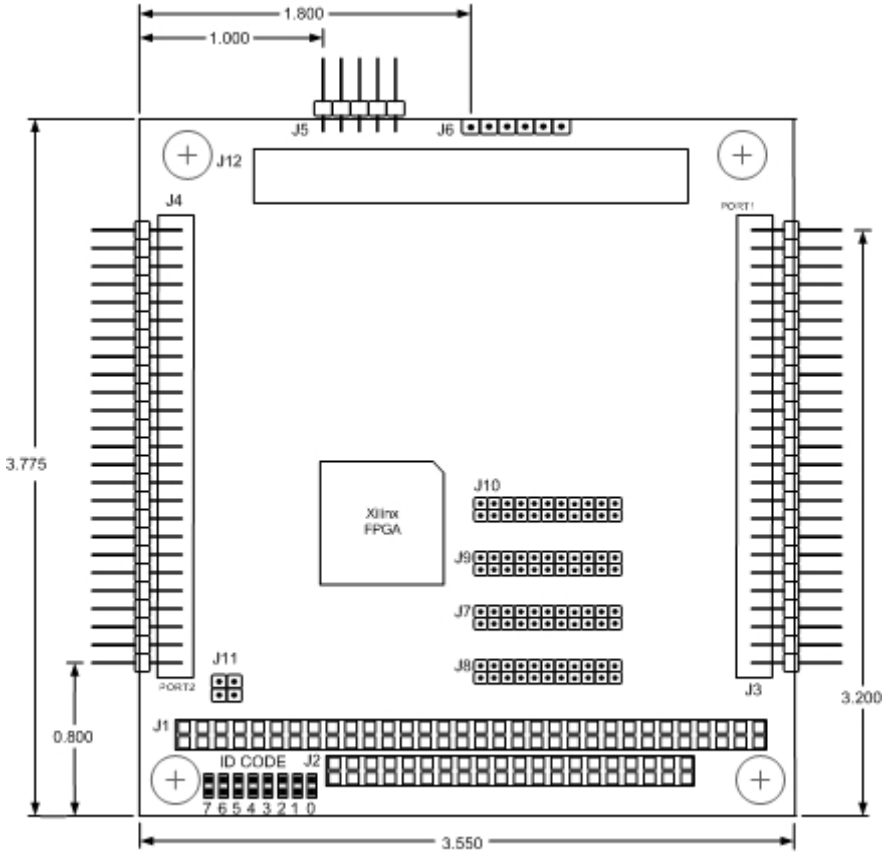
Enhanced Features

- On-board EEPROM for user configuration data storage.
- An LED display for easy identification of FPGA personality, which can also be read in a register.
- Interrupt source selection, with counter/timer, DIO or external line options.
- Four-channel auxiliary DIO for additional general-purpose I/O.
- A register-accessible FPGA revision code for version control.
- Software-controlled board reset.

Board Layout

Board Drawing

Figure 1: GPIO-MM-12 Board Layout



I/O Connector Pinout

Digital I/O Header Pinout

Connector (J4) is the 50-pin general-purpose DIO interface. The connector connects directly to the FPGA, which implements the functionality of a 82C55A PPI chips. This gives a total of 48 bidirectional DIO lines.

The J4 pins can be configured to pull-up to +5V or pull-down to ground using jumper J11, as described in Section 4, Board Configuration, Line Pull-up/pull-down Selection.

Port 1A7	1	2	Port 2A7
Port 1A6	3	4	Port 2A6
Port 1A5	5	6	Port 2A5
Port 1A4	7	8	Port 2A4
Port 1A3	9	10	Port 2A3
Port 1A2	11	12	Port 2A2
Port 1A1	13	14	Port 2A1
Port 1A0	15	16	Port 2A0
Port 1B7	17	18	Port 2B7
Port 1B6	19	20	Port 2B6
Port 1B5	21	22	Port 2B5
Port 1B4	23	24	Port 2B4
Port 1B3	25	26	Port 2B3
Port 1B2	27	28	Port 2B2
Port 1B1	29	30	Port 2B1
Port 1B0	31	32	Port 2B0
Port 1C7	33	34	Port 2C7
Port 1C6	35	36	Port 2C6
Port 1C5	37	38	Port 2C5
Port 1C4	39	40	Port 2C4
Port 1C3	41	42	Port 2C3
Port 1C2	43	44	Port 2C2
Port 1C1	45	46	Port 2C1
Port 1C0	47	48	Port 2C0
+5V	49	50	Ground

NOTE: The connector is labeled "Port 2," which should not be confused with DIO ports A, B and C and the fixed-direction TTL ports.

Signal	*Description*
Port 1A0-Port 1A7	8255-1 Port A, bits 0-7
Port 1B0-Port 1B7	8255-1 Port B, bits 0-7
Port 1C0-Port 1C7	8255-1 Port C, bits 0-7
Port 2A0-Port 2A7	8255-2 Port A, bits 0-7
Port 2B0-Port 2B7	8255-2 Port B, bits 0-7
Port 2C0-Port 2C7	8255-2 Port C, bits 0-7
+5V	+5 volt DC from the PC/104 bus.
Ground	Digital ground from the PC/104 bus.

Counter/timer Header Pinout

Connector (J3) is the 50-pin counter/timer interface. The connector connects directly to the FPGA, which implements the functionality of two CTS9513 counter/timer chips.

- Ten input and ten output counter/timer signals
- Eight input and eight output TTL-level signals
- Ten gates
- Power and ground

The J3 pins may be configured to pull-up to +5V or pull-down to ground using jumper J8, as describe in Section 4, Board Configuration, Line Pull-up/pull-down Selection.

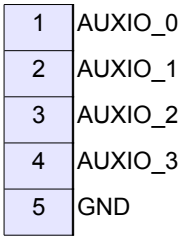
In1	1	2	In2
Gate1	3	4	Gate2
Out1	5	6	Out2
In3	7	8	In4
Gate3	9	10	Gate4
Out3	11	12	Out4
In5	13	14	Out5
Gate5	15	16	FOUT
In6	17	18	In7
Gate6	19	20	Gate7
Out6	21	22	Out7
In8	23	24	In9
Gate8	25	26	Gate9
Out8	27	28	Out9
In10	29	30	Out10
Gate10	31	32	Interrupt In
DOUT7	33	34	DIN7
DOUT6	35	36	DIN6
DOUT5	37	38	DIN5
DOUT4	39	40	DIN4
DOUT3	41	42	DIN3
DOUT2	43	44	DIN2
DOUT1	45	46	DIN1
DOUT0	47	48	DIN0
+5V	49	50	Ground

NOTE: The connector is labeled "Port 1," which should not be confused with DIO ports A, B and C and the fixed-direction TTL ports.

Signal	*Description*
In1-In10	Ten external clock source lines that may be associated with one of the ten internal counters or FOUT.
Out1-Out10	Ten tri-state outputs lines associated with one of the ten internal counters. These may be programmed for pulse, wave or complex duty cycle waveforms.
Gate1-Gate10	Ten input lines used to control counter behavior. These may also be used as clock or count input sources for the internal counters or the FOUT divider.
FOUT	FOUT is a general-purpose, auxiliary clock output derived from the 9513 input clock using a programmable divider.
Interrupt In	External interrupt for external PC/104 bus hardware interrupt operation.
DOUT0-DOUT7	Eight general-purpose digital output lines.
DIN0-DIN7	Eight general-purpose digital input lines.
+5V	+5 volt DC from the PC/104 bus.
Ground	Digital ground from the PC/104 bus.

Auxiliary I/O Header Pinout

The auxiliary I/O header (J5) is provided for bidirectional, TTL-level, general-purpose I/O.



Card Voltage Type	*Pin Configuration*
AUXIO_0-AUXIO_3	Four bidirectional, TTL-level, general-purpose I/O signals.
GND	Ground

Board Configuration

Base Address Selection

Jumper J10, positions 2-5, is used to configure the base address of the DIO (8255) registers. The 8255 register map occupies 8 bytes of I/O address space, as described in Section 5, I/O Map.

Jumper positions 6-9, is used to configure the base address of the counter/timer I/O (9513) registers and the enhanced features registers. The 9513 register map occupies 16 bytes of I/O address space, as described in Section 5, I/O Map.

Jumper the locations as shown to set the 8255 and 9513 base addresses.

I/O	***2***	***3***	***4***	***5***	◄ ***DIO Pins***
Address	***6***	***7***	***8***	***9***	◄ ***C/T Pins***
0040h	Out	In	In	In	
0080h	In	Out	In	In	
00C0h	Out	Out	In	In	
0100h	In	In	Out	In	
0140h	Out	In	Out	In	
0180h	In	Out	Out	In	
01C0h	Out	Out	Out	In	
0200h	In	In	In	Out	
0240h	Out	In	In	Out	
0280h	In	Out	In	Out	
02C0h	Out	Out	In	Out	
0300h	In	In	Out	Out	
0340h	Out	In	Out	Out	
0380h	In	Out	Out	Out	
03C0h	Out	Out	Out	Out	

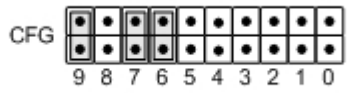
NOTE: Different address must be selected for the DIO and counter/timer functions.

The example, below, selects a DIO base address of 0040h.

Figure 2: Set DIO Base Address to 0040h

The following example selects a counter/timer base address of 0100h.

Figure 3: Set Counter/Timer Base Address to 0100h

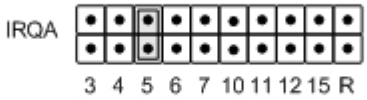


Interrupt Level Selection

Jumper J7 is used to switch the IRQA interrupt and jumper J9 is used to switch the IRQB interrupt. PC/104 lines that can be selected are IRQ3 to IRQ7, IRQ10 to IRQ12 and IRQ15. (The examples shown below also apply to the J9 jumper block for IRQB).

The example, below, shows J7 jumpered to route IRQA to PC/104 IRQ5.

Figure 4: Route IRQA to PC/104 IRQ5

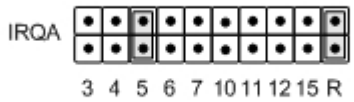


Jumper blocks J7 and J9 are also used to enable interrupt sharing for each IRQ signal, enabling a 1KΩ pull-down resistor.

When an I/O module drives an IRQ line, its output signal must either drive logic high, or become a tri-state input. This allows more than one device to be on a single IRQ line. To facilitate this, a pull-down resistor is used on the IRQ line to bring the logic low when no device is signaling an interrupt. Shorting the "R," resistor, jumper connects a 1K pull-down resistor between the IRQ line and ground.

The following example shows IRQA connected to a 1K pull-down resistor and routed to IRQ5, which is shared.

Figure 5: Connect IRQA to Pull-down Resistor, Route to Shared IRQ5



NOTE: There can only be one pull-down resistor per IRQ line. If jumper blocks J7 and J9 both select IRQ5, only one jumper block should have the R-jumper inserted. Likewise, there should only be one R-jumper in a configuration of multiple GPIO-MM-12 boards.

NOTE: All positions are paralleled with zero-ohm resistor locations for hard-wire configuration.

IRQA and IRQB interrupts sources are selected by configuring the enhanced feature register, 0Ch, as described in the Section 6, Register Bit Descriptions, Interrupt Source Register.

NOTE: All positions are paralleled with zero-ohm resistor locations for hard-wire configuration line pull-up/pull-down selection.

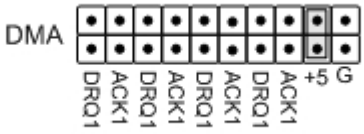
I/O Line Pull-up/Pull-down Selection

Use jumper J8 to configure the pull-up and pull-down state of the counter/timer header pins (J3). Use jumper J11 to configure the pull-up and pull-down state of the DIO header pins (J4).

DIO pin pull-up and pull-down state is configured as shown in the following examples.

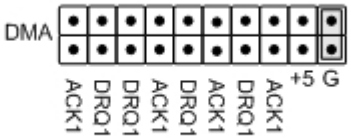
Jumper the position marked "+5" to pull the J3 I/O pins up to +5VDC.

Figure 6: Pull I/O Pins Up to +5VDC



Jumper the position marked "G" to pull the J3 I/O pins down to ground.

Figure 7: Pull I/O Pins Down to Ground



NOTE: Placing a jumper on both "+5" and "G" simultaneously will short the +5VDC power plane to ground.

I/O Map

Overview

The register base address is determined by setting jumper J10, as described in Section 4, Board Configuration, Base Address Selection. Jumper pins 2-5 set the DIO base address and pins 6-9 set the counter/timer base address.

Counter/Timer and Enhanced Feature Programming

Sixteen registers are used for counter/timer and enhanced feature programming.

Offset	*Description*
00h	9513-1 command and status data register. Transfers command and status data to/from the register pointed to at base+01h.
01h	9513-1 command and status data register pointer. Address of the command and status registers for transferring the 8-bit data located at base+00h.
02h	8-bit DIO data. Set or read the 9513 DIO lines.
03h	Shadow register of base+02h.
04h	9513-2 command and status data register. Transfers command and status data to/from the register pointed to at base+05h.
05h	9513-2 command and status data register pointer. Address of the command and status registers for transferring the 8-bit data located at base+04h.
06h	Interrupt control. Enable and reset counter/timer interrupts.
07h	Shadow register of base+06h.
08h	EEPROM data. Data written to and read from the EEPROM.
09h	EEPROM address. The EEPROM location for reading or writing data.
0Ah	EEPROM control and status register. Initiate EEPROM data transfer and set the data transfer direction. Also, indicates when valid data is available from EEPROM during a read operation.
0Bh	FPGA revision code. Get the on-board FPGA program revision level.
0Ch	Interrupt source selection. Specify the interrupt source for IRQA/IRQB.
0Dh	Interrupt control and status. Enable, disable and clear IRQA/IRQB interrupts and gets the IRQA/IRQB interrupt status.
0Eh	Auxiliary DIO control and status. Set the state of the auxiliary DIO lines and read the current DIO line state.
0Fh	Board reset and board ID code. Reset the board or get the FPGA personality ID code.

DIO Programming

Eight registers are used for DIO programming.

Offset	*Description*
00h	8255-1 port A DIO register
01h	8255-1 port B DIO register
02h	8255-1 port C DIO register
03h	8255-1 control and status register
04h	8255-2 port A DIO register
05h	8255-2 port B DIO register
06h	8255-2 port C DIO register
07h	8255-2 control and status register

Register Bit Descriptions

Refer to the I/O Map for counter/timer and DIO register sets.

9513 Command and Status Data

Counter/timer Base+00h (9513-1), Base+04h (9513-2)

Bit:	7	6	5	4	3	2	1	0
Name:	D7	D6	D5	D4	D3	D2	D1	D0

D7-D0 Counter/timer command and status data for the 9513. These data are written to or read from the counter/timer command and status register at the location specified by the command and status register pointer (base+01h). Refer to the 9513 data sheet, Additional Information, for a description of the command and status registers.

9513 Command and Status Data Pointer Registers

Counter/timer Base+01h (9513-1), Base+05h (9513-2)

Bit:	7	6	5	4	3	2	1	0
Name:	PTR							

PTR Counter/timer command and status register pointer for the 9513. This register points to the 9513 command and status register location to write the data contained in the Command and Status Data Register (base+00h). Refer to the 9513 datasheet, Additional Information, for a description of the command and status register.

9513 DIO Data Registers

Bit:	7	6	5	4	3	2	1	0
Name:	DIO7IN DIO7OUT	DIO6IN DIO6OUT	DIO5IN DIO5OUT	DIO4IN DIO4OUT	DIO3IN DIO3OUT	DIO2IN DIO2OUT	DIO1IN DIO1OUT	DIO0IN DIO0OUT

DIO0IN-DIO7IN DIO input line state. Reading the bit corresponding to the DIO line returns the line state.
0 = low level line state
1 = high level line state

DIO0OUT-DIO7OUT DIO output line state. Writing the bit corresponding to the DIO line sets the line state.
0 = set line state to low level
1 = set line state to high level

9513 Interrupt Control Registers

Counter/timer Base+06h, Base+07h (shadow register)

Bit:	7	6	5	4	3	2	1	0
Name:	-							INTE

INTE Interrupt enable. Write to this bit to enable or disable counter/timer interrupts.
0 = disable interrupts
1 = enable interrupts
If IRQA and IRQB are both counter/timer interrupts, both interrupts are enabled or disabled by writing to this register.
IRQA and IRQB are considered counter/timer interrupts if the interrupt source is the counter/timer output 1-10, dedicated interrupt input, or DIO input 0.
This is equivalent to the IRQAEN/IRQBEN and IRQADIS/IRQBDIS bits of the Interrupt Control/Status Register (base+0Dh).

EEPROM Data Register

Counter/timer Base+08h

Bit:	7	6	5	4	3	2	1	0
Name:	D7	D6	D5	D4	D3	D2	D1	D0

D7-D0 Writing to this register writes data to the EEPROM at the address specified by the EEPROM Address Register (base+09h). Reading from this register returns the EEPROM data at the EEPROM Address Register (base+09h) location; read data is valid when EEBUSY = 0 in the EEPROM Status Register (base+0Ah).

EEPROM Address Register

Counter/timer Base+09h

Bit:	7	6	5	4	3	2	1	0
Name:	A7	A6	A5	A4	A3	A2	A1	A0

A0-A7 EEPROM address. This register specifies the EEPROM address to read/write the data in the EEPROM Data Register (base+08h). The address range is 0 to 256.

EEPROM Control and Status Register

Counter/timer Base+0Ah

Bit:	7	6	5	4	3	2	1	0
Name:	EE_EN	EE_RW	EEBUSY	-				

EEBUSY — EEPROM busy status indicator. When reading data from the EEPROM, the data is valid when this bit indicates the EEPROM is not busy.
0 = EEPROM is not busy.
1 = EEPROM is busy. Wait before accessing EEPROM.

EE_RW — EEPROM data transfer direction. Read or write the EEPROM at the EEPROM address in the Address Register (base+09h).
0 = Write
1 = Read

EE_EN — EEPROM enable. Set bit to 1 to initiate an EEPROM byte transfer in the direction indicated by the EE_RW bit.

FPGA Revision Code Register

Counter/timer Base+0Bh

Bit:	7	6	5	4	3	2	1	0
Name:	FPGA Revision Code							

FPGA Revision Code — This register contains a hexadecimal FPGA revision code. The initial value is 12h.

Interrupt Source Register

Counter/timer Base+0Ch

Bit:	7	6	5	4	3	2	1	0
Name:	IRQB				IRQA			

IRQA Select the IRQA interrupt source:
00h = Counter/timer 1 output
01h = Counter/timer 2 output
02h = Counter/timer 3 output
03h = Counter/timer 4 output
04h = Counter/timer 5 output
05h = Counter/timer 6 output
06h = Counter/timer 7 output
07h = Counter/timer 8 output
08h = Counter/timer 9 output
09h = Counter/timer 10 output
0Ah = dedicated interrupt input pin ◄ (Reset value)
0Bh = DIO input 0
0Ch = 8255-1 C0
0Dh = 8255-1 C3
0Eh = 8255-2 C0
0Fh = 8255-2 C3

IRQB Select the IRQB interrupt source, using the same values as for IRQA, above. The reset value for IRQB is 0Ch.

Interrupt Control and Status Register

Counter/timer Base+0Dh

Bit:	7	6	5	4	3	2	1	0
Name:	-	IRQBEN	IRQBDIS	IRQBSTS IRQBCLR	-	IRQAEN	IRQADIS	IRQASTS IRQACLR

IRQASTS / IRQACLR — IRQA interrupt status and reset. A value of 1 when reading this register bit (IRQASTS) indicates an IRQA interrupt occurred. Write a value of 1 to this bit (IRQACLR) to clear the interrupt.

IRQADIS — IRQA interrupt disable. Write a value of 1 to this bit to disable the IRQA interrupt. This is equivalent to the INTE bit of the Interrupt Control Register (base+0Dh).

IRQAEN — IRQA interrupt enable. Write a value of 1 to this bit to enable the IRQA interrupt. This is equivalent to the INTE bit of the Interrupt Control Register (base+0Dh).

IRQBSTS / IRQBCLR — IRQB interrupt status and reset. A value of 1 when reading this register bit (IRQBSTS) indicates an IRQB interrupt occurred. Write a value of 1 to this bit (IRQBCLR) to clear the interrupt.

IRQBDIS — IRQB interrupt disable. Write a value of 1 to this bit to disable the IRQB interrupt. This is equivalent to the INTE bit of the Interrupt Control Register (base+0Dh).

IRQBEN — IRQB interrupt enable. Write a value of 1 to this bit to enable the IRQB interrupt. This is equivalent to the INTE bit of the Interrupt Control Register (base+0Dh).

Auxiliary DIO Control and Status Register

Counter/timer Base+0Eh

Bit:	7	6	5	4	3	2	1	0
Name:	AUX3DIR	AUX2DIR	AUX1DIR	AUX0DIR	AUX3IN AUX3OUT	AUX2IN AUX2OUT	AUX1IN AUX1OUT	AUX0IN AUX0OUT

AUXnIN / AUXnOUT — Auxiliary DIO line. Read the respective AUXnIN bit to determine the auxiliary DIO line state.
0 = low level
1 = high level
If the line is currently set to output mode, according to the AUXnDIR bit, below, the read value corresponds to the current output level.
Write the low-level or high-level value to the AUXnOUT bit to set the respective auxiliary DIO line level. The level applies even if the line direction, AUXnDIR, is set to input mode. The value will be applied when the line direction is set to output mode.

AUXnDIR — Auxiliary line I/O direction and state. Write the following values to the AUXnDIR bit to set the I/O direction (output/input) for the respective auxiliary DIO line.
0 = output mode
1 = input mode
Read the bit to determine the current I/O mode.

Board Reset and ID Register

Counter/timer Base+0Fh

Bit:	7	6	5	4	3	2	1	0
Name:	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0 BRDRST

ID0-ID7 FPGA personality ID. Indicates the personality of the onboard FPGA; the value for the GPIO-MM-12 board type is 11h.

BRDRST Board reset. Write 1 to this bit to reset the board, which has the same affect as an external reset pulse.

8255 Data Registers

DIO Base+00h (8255-1 Port A), DIO Base+04h (8255-2 Port A)
DIO Base+01h (8255-1 Port B), DIO Base+05h (8255-2 Port B)
DIO Base+02h (8255-1 Port C), DIO Base+06h (8255-2 Port C)

Bit:	7	6	5	4	3	2	1	0
Name:	DATA							

DATA 8-bit parallel data. On reset, the port is set to input mode and the port is held at a logic level 1 until the reset signal is removed. The port remains in input mode until changed using the control register. Following a reset, all lines are set to input mode.

8255 Control and Status Registers (Basic Mode Definition – MSFLAG=1)

DIO Base+03h (8255-1), DIO Base+07h (8255-2)

Bit:	7	6	5	4	3	2	1	0
Name:	MSFLAG	MSELA		PADIR	PCUDIR	MSELB	PBDIR	PCLDIR

PCLDIR Port C (lower) direction. Sets the direction of the port C I/O signals 0-3.
0 = output
1 = input ◄ (Reset value)

PBDIR Port B direction. Sets the direction of the port B I/O signals.
0 = output
1 = input ◄ (Reset value)

MSELB Group B mode selection. Sets the mode of operation for the group B signals.
0 = mode 0 ◄ (Reset value)
1 = mode 1
NOTE: 1. Only mode 0 is currently implemented.
2. All output registers are reset when the mode is changed.

PCUDIR Port C (upper) direction. Sets the direction of the port C I/O signals 4-7.
0 = output
1 = input ◄ (Reset value)

PADIR Port A direction Sets the direction of the port A I/O signals.
0 = output
1 = input ◄ (Reset value)

MSELA Group A mode selection. Sets the mode of operation for the group B signals.
00h = mode 0 ◄ (Reset value)
01h = mode 1
1xh = mode
NOTE: 1. Only mode 0 is currently implemented.
2. All output registers are reset when the mode is changed.

MSFLAG Mode set flag. Selects the port configuration mode.
0 = Bit set/reset control register mode
When MSFLAG is reset, this register is used to set/reset individual Port C bits.
1 = Basic mode definition control register mode ◄ (Reset value)
When MSFLAG is set, this register is used for direction and mode selection.
NOTE: When the control word is read, the value of MSFLAG is always 1, implying basic control word information is being read.

8255 Control and Status Registers (Bit SET/RESET Mode – MSFLAG=0)

DIO Base+03h (8255-1), DIO Base+07h (8255-2)

Bit:	7	6	5	4	3	2	1	0
Name:	MSFLAG	-			BSEL			SET

SET Bit set/reset individual command.
0 = reset
1 = set

BSEL Port C bit select.
0 = bit 0
1 = bit 1
2 = bit 2
3 = bit 3
4 = bit 4
5 = bit 5
6 = bit 6
7 = bit 7

MSFLAG Mode set flag. Selects the port configuration mode.
0 = Bit set/reset control register mode
When MSFLAG is reset, this register is used to set/reset individual Port C Bits.
1 = Basic mode definition control register mode
When MSFLAG is set, this register is used for direction and mode selection.
NOTE: When the control word is read, the value of MSFLAG is always 1, implying basic control word information is being read.

Programming the Counter/Timer

Overview

To program the 9513 effectively and take advantage of its myriad features requires an understanding of its structure and operation. A datasheet on the 9513 is included at the end of this manual.

Review pages four (starting with "Functional Description") through 11 to understand the structure of the 9513 chip and its capabilities. The various counter operating modes are described starting on page 13. A few explanatory notes are given below.

Accessing the Counter/Timer Internal Registers

The chip contains many internal registers. To minimize the I/O memory footprint, a data pointer scheme is used to access these registers. This scheme is reflected in the GPIO-MM-12 board's I/O map (Section 5, I/O Map). The data pointer values are shown in the 9513 datasheet on page 8, Table 4. The appropriate data pointer value is written to the data pointer register for the chip (Base + 1 for chip no. 1 and Base + 5 for chip no. 2). Then the register is accessed through the data register (Base + 0 for chip no. 1 and Base + 4 for chip no. 2).

Master Mode Register

Each chip contains a Master Mode Register that defines global characteristics for the chip. Note the bit that controls the data bus width. This should always be set to 0 for 8-bit bus access on GPIO-MM-12.

Counter Mode Register

Each chip contains five Counter Mode Registers; one for each counter. This register is used to program the operating mode of the counter, including input source, gating method, output type, load/reload behavior and count direction. Note that in the Gate description, Gate N means the gate for the counter being programmed, and Gate N-1 means the gate for the previous counter. Gate N-1 is not valid for counter 1 (or counter 6 on GPIO-MM-12, since that corresponds to counter 1 on the second chip).

Counter Modes

Each combination of Gate control, Repetition, Reload source, and Special gate are given a letter mode name. See the counter mode tables on page 13 of the datasheet. The behavior of these modes as well as their timing diagrams are given starting on page 14 of the datasheet. Please, note the errata on page 12 of the datasheet.

FOUT Frequency Output

A programmable frequency generator circuit is provided for the counter/timer, and is described in the 9513 datasheet. It has an input source, a multi-stage decimal or BCD divider, and a user-programmable divider. All options are programmed through the Master Mode Register. The FOUT circuit of the 9513-1 is available on the FOUT pin on the GPIO-MM-12 board's I/O header. Its source can be the input or gate from counters 1-5 or any of the five internal frequency dividers built into the chip and driven by the clock. The FOUT circuit of the 9513-2 is not available externally.

Counter Commands

A set of commands is used to control the counters. These are described in the 9513 datasheet. The Diamond Systems Universal Driver software provides full support for the various 9513 functions.

Counter Programming

Before programming any individual counter, the 9513 Master Mode Register must be programmed. Programming an individual counter requires several steps. First, the Counter Mode Register must be set to indicate the desired operating characteristics of the counter, such as gating level and type, count direction and type, and output type.

After the Counter Mode Register is programmed, load the appropriate data into the Load and/or Hold register(s). The Load register is used to set the divide-by-n and initial count values. The Hold register may also be required for certain counter modes, such as variable-duty-cycle square wave functions.

You may optionally want to set the initial output level.

If you are using counters 1 or 2 in alarm mode, the alarm register must also be programmed.

Next, load the initial count into the Count register using the Load command.

Finally, "arm", or enable, the counter using the Arm command.

To read a counter, issue a Save command. This stores the counter's current contents in the Hold register. Then, read the Hold register.

A counter can be armed or disarmed, and its current contents can be saved, at any time under software control through these commands.

The information below summarizes the procedure for programming a counter:

To set up counter operation:

1. Program the Master Mode Register.
2. Program the Counter Mode Register.
3. Load initial data into the Load Register.
4. (Optional) Load initial data into the Hold Register.
5. Issue a Load and Arm command for the counter.

To read counter contents:

1. Issue a Save or Disarm and Save command.
2. Read the Hold Register.

Programming Digital I/O

48-bit Programmable Direction (8255)

GPIO-MM-12 provides 48 DIO lines using an FPGA core implementation of two 82C55A devices (82C55A-1 and 82C55A-2). The DIO functionality includes 48 programmable direction lines, and 8 fixed inputs and 8 fixed outputs. The 48 programmable I/O lines are buffered for enhanced output current, while the fixed I/O and the counter/timer signals feature ESD-protective circuitry. All I/O lines contain jumper-selectable 10Kohm pull-up/pull-down resistors.

Operation of the 82C55A FPGA core should be as described in the 82C55A PPI datasheet. Refer to the 82C55A datasheet, Additional Information, for detailed register and programming information.

The 82C55A has three parallel I/O ports. Ports A and B are 8-bit bi-directional I/O ports. Port C is divided into two 4-bit bi-directional I/O ports. For programming, the ports are arranged into two groups, as shown below.

Port Group	***Description***
A	8 bits of Port A and upper 4 bits (4-7) of port C.
B	8 bits of Port B and lower 4 bits (0-3) of port C.

NOTE: The port groups can be separately configured for different operating modes. However, GPIO-MM-12 only implements operating mode 0, which provides simple, bidirectional I/O without handshaking.

Port C bits may be individually set and reset by setting the MSFLAG in the 8255 Control and Status Register and programming the remaining register bits for the desired bit state.

Setting the 8255 Control and Status Register to the following values gives 16 possible I/O configurations.

Status and Control Register Bits				***Group A***		***Group B***	
PADIR	PCUDIR	PBDIR	PCLDIR	Port A	Port C (upper)	Port B	Port C (lower)
0	0	0	0	Output	Output	Output	Output
0	0	0	1	Output	Output	Output	Input
0	0	1	0	Output	Output	Input	Output
0	0	1	1	Output	Output	Input	Input
0	1	0	0	Output	Input	Output	Output
0	1	0	1	Output	Input	Output	Input
0	1	1	0	Output	Input	Input	Output
0	1	1	1	Output	Input	Input	Input
1	0	0	0	Input	Output	Output	Output
1	0	0	1	Input	Output	Output	Input
1	0	1	0	Input	Output	Input	Output
1	0	1	1	Input	Output	Input	Input
1	1	0	0	Input	Input	Output	Output
1	1	0	1	Input	Input	Output	Input
1	1	1	0	Input	Input	Input	Output
1	1	1	1	Input	Input	Input	Input

16-bit Fixed Direction (9513)

Connector J3 has 8 fixed TTL inputs and 8 fixed TTL outputs. The outputs are set by writing to base+2 or 3. (See 9513 DIO Data Registers). Write an 8-bit value to the register at base+2 (or base+3) to immediately output the value to the 8 output lines. When reading register base+2 (or base+3), the FPGA returns the logic state of the 8 input lines.

Programming Enhanced Features

EEPROM Programming

The EEPROM provides non-volatile memory for storing application data.

Program the EEPROM using the following steps. Repeat these steps for each data byte.

1. Write the data byte to the EEPROM Data Register (08h).
2. Specify the EEPROM address (0-256) where the data is to be written by writing the address to the EEPROM Address Register (09h).
3. Set the data transfer direction to write by resetting the EE_RW bit in the EEPROM Control and Status Register (0Ah).
4. Set the EE_EN bit in the EEPROM Control and Status Register (0Ah) to initiate the write operation.

To read stored EEPROM data, use the following steps. Repeat these steps for each data byte.

1. Specify the EEPROM address (0-256) where the data is to be read from by writing the address to the EEPROM Address Register (09h).
2. Set the data transfer direction to read by setting the EE_RW bit in the EEPROM Control and Status Register (0Ah).
3. Reset the EE_EN bit in the EEPROM Control and Status Register (0Ah) to initiate the read operation.
4. Test the EEPROM Control and Status Register (0Ah) EEBUSY bit to determine that the data transfer has completed. When EEBUSY is zero, a valid data byte is available and the next byte may be read.

Specifications

General Specifications

- Base FPGA: Xilinx Spartan II, 200,000 gates, 40K RAM bits
- Input clock: 40MHz
- FPGA code storage: Flash memory, field upgradeable via JTAG
- ID indicator: 8-bit LED display indicates FPGA code personality; field upgradeable via JTAG
- Counter/timers: 10, 16 bits, using 2 CTS9513 cores
- Maximum counting frequency: 40MHz
- Counter modes: Counter, rate/square-wave generator, pulse-width modulator, programmable one-shot, hardware/software triggered strobe
- Programmable I/O: 48, using 2 82C55A cores
- Fixed direction I/O: 8 fixed inputs, 8 fixed outputs
- Output current, buffered I/O: Logic 0: 64mA max per line buffered I/O; Logic 1: -15mA max per line
- Output current, fixed I/O and counter/ timers: ±24mA max
- Dimensions: 3.55" x 3.775", PC/104 form factor
- PC/104 bus: 16-bit stackthrough ISA bus
- Power supply: +5VDC ±5%
- Operating temperature: -40° to +85° C
- Weight: 2.2oz

Additional Information

Datasheets

Datasheets provide programming reference information for the counter/timer and DIO functions.

1. CTS9513-2 5Chan 16 bit 20MHz Counter/Timer, Celeritous Technical Services Corp., September 2000
2. 82C55A CMOS Programmable Peripheral Interface, Harris Semiconductor, March 1997

Technical Support

For technical support, please email support@diamondsystems.com or contact Diamond Systems Corporation technical support at 1-650-810-2500.